Amendments to the Claims

Please cancel claim 1 as indicated below. A listing of the pending claims follows. This listing of claims replaces all prior versions, and listings of claims in the application.

Listing of Claims:

1-21. (cancelled)

22. (previously presented) A power-on reset circuit in a flash EPROM memory comprising:

a first capacitor with one terminal grounded and the other terminal connected to a first node;

a first resistor with one terminal tied to V_{DD} and the other terminal tied to said first node;

a plurality of inverters wherein the input of said plurality of said inverters is connected to said first node and the output of said plurality of inverters is connected to the circuit output;

a latch comprised of a first and second inverter wherein the input of said first inverter and the output of said second inverter are connected to said first node and the input of said second inverter and the output of said first inverter are connected to a second node;

a second capacitor with one terminal connected to V_{DD} and the other terminal connected to said second node;

a first MOSFET with the drain terminal connected to said second node, the source terminal connected to ground and the gate terminal connected to a third node;

a second resistor with one terminal connected to said third node and the other terminal connected to ground;

a third resistor with one terminal connected to said third node and the other terminal connected to a fourth node; and

a second MOSFET with the drain terminal connected to V_{DD}, the source terminal connected to said fourth node and the gate terminal connected to said circuit output.

23. (previously presented) The circuit according to Claim 22 wherein said first capacitor is a MOSFET device.

24. (previously presented) The circuit according to Claim 22 wherein said second capacitor is a MOSFET device.

25. (previously presented) The circuit according to Claim 22 wherein said first resistor is a MOSFET device.

26. (previously presented) The circuit according to Claim 22 wherein erasing of reference cells in said flash EPROM memory is initiated by a pulse generated by said power-on reset circuit upon each application of supply voltage to said flash EPROM.

27. (previously presented) The circuit according to Claim 26 wherein said pulse has duration of between about 0.1 and 10mS.

28. (previously presented) The circuit according to Claim 27 wherein said duration of said pulse is determined by the values of one capacitor and one resistor.

29. (previously presented) The circuit according to Claim 28 wherein said capacitor is a MOSFET device.

30. (previously presented) The circuit according to Claim 28 wherein said resistor is a MOSFET device.

31. (previously presented) A power-on reset circuit in a flash EPROM memory comprising:

a first capacitor with one terminal grounded and the other terminal connected to a first node;

a first resistor with one terminal tied to V_{DD} and the other terminal tied to said first node;

an odd plurality of inverters wherein the input of said odd plurality of said inverters is connected to said first node and the output of said odd plurality of inverters is connected to the power-on reset circuit output;

a latch comprised of a first and second inverter wherein the input of said first inverter and the output of said second inverter are connected to said first node and the input of said second inverter and the output of said first inverter are connected to a second node;

a second capacitor with one terminal connected to V_{DD} and the other terminal connected to said second node;

a first MOSFET with the drain terminal connected to said second node, the source terminal connected to ground and the gate terminal connected to a third node;

a second resistor with one terminal connected to said third node and the other terminal connected to ground;

a third resistor with one terminal connected to said third node and the other terminal connected to a fourth node; and

a second MOSFET with the drain terminal connected to V_{DD}, the source terminal connected to said fourth node and the gate terminal connected to said power-on reset circuit output.

32. (previously presented) The circuit according to Claim 31 wherein said first capacitor is a MOSFET device.

33. (previously presented) The circuit according to Claim 31 wherein said second capacitor is a MOSFET device.

34. (previously presented) The circuit according to Claim 31 wherein said first resistor is a MOSFET device.

35. (previously presented) The circuit according to Claim 31 wherein erasing of reference cells in said flash EPROM memory is initiated by a pulse generated by said power-on reset circuit upon each application of supply voltage to said flash EPROM.

36. (previously presented) The circuit according to Claim 35 wherein said pulse has duration of between about 0.1 and 10mS.

37. (previously presented) The circuit according to Claim 35 wherein said duration of said pulse is determined by the values of one capacitor and one resistor.

38. (previously presented) The circuit according to Claim 35 wherein said capacitor is a MOSFET device.

39. (previously presented) The circuit according to Claim 35 wherein said resistor is a MOSFET device.